Disclaimer
This syllabus is to be used as a guideline only. The information provided is a summary of topics to be covered in the class.
Information contained in this document such as assignments, grading scales, due dates, office hours, required books and materials may be from a previous semester and are subject to change. Please refer to your instructor for the most recent version of the syllabus.

EEE598 ST: Serial Links

Instructor: Dr. Hongjiang Song hongjiang.song@asu.edu

Credits: 4 hours
Prerequisites:
- Basic VLSI analog circuits
- Basic VLSI digital circuits

Grading:

Homework	15%
Midterm Exams	40%
Final Exam	25%
Project	20%

Course Description:
This course was originally known as the VLSI High-Speed I/O Circuits. It covers various VLSI circuit design topics of VLSI high-speed I/O (or broadband) circuits including the theoretical basis, design, modeling, and validation techniques. This course is intended for first or second year graduate students and the objective is to build a practical knowledge of the VLSI high-speed I/O circuits and the applications to various industry high-speed I/O circuit standards, such as LVDS, USB2.0, 1394, S-ATA, PCI-Express, Mipi, etc. There will be weekly (bi-weekly) HW and design projects. CAD tools such as CADENCE, MATLAB will be used during the class.

Text book:
- "VLSI High-Speed I/O Circuits – Theoretical Basis, Circuit Architectures, Behavioral Modeling and Circuit Implementations" by Dr. Hongjiang Song. http://www2.xlibris.com/bookstore/bookdisplay.aspx?bookid=62861

Reference:
- "VLSI High-Speed I/O Circuits - Problems, Projects, and Questions" by Hongjiang Song. http://www.lulu.com/shop/hongjiang-song/vlsi-high-speed-io-circuits-problems-projects-and-questions/paperback/product-21489290.html
- Selected journal/conference papers on VLSI High-Speed I/O Circuits that support covered topics

Lecture Topics:
- High-Speed I/O Circuit Fundamental
  1. High-speed I/O standards, trends and fundamental design challenges
  2. Basic I/O prototype and SFG models, Basic I/O circuit timing equation
  3. I/O circuit architectures, Common Clock, Forward Clock, and Embedded Clock Signaling
- High-Speed Serial I/O Modeling
  1. Jitter analysis, modeling and link jitter budgeting
  2. Bit Error Rate (BER) analysis and modeling
  3. DRC tracking loop modeling
  4. PLL/DLL/PI modeling
  5. Signal Integrity and Power Delivery
- VLSI High-Speed Serial I/O Circuit designs/implementations
  1. Transmitter circuits
  2. Receiver circuits
  3. Channel, T-line, Automatic Termination and Equalization Circuits
  4. PLL/DLL/PI circuits
  5. Data recovery circuit
  6. Voltage and current references circuits
- Validation Techniques of High-Speed I/O Circuits
  1. TDR & VNA
  2. Jitter & BERT measurement