Arizona State University

EEE 523: Advanced Analog IC Design

Course and Faculty Information

Course Description: Analysis and design of analog integrated circuits: analog circuit blocks, reference circuits, operational-amplifier circuits, feedback, and nonlinear circuits.

Credits: 4

Class Schedule and Location: T / TH 10:30 am - 11:45 am Room: Tempe - LSEB04

Prerequisites: EEE 433 - This is a firm requirement! Please Do Not take 523 if you have not taken 433 at ASU or an equivalent. If you don't know what equivalent means, please check with 433 syllabus. 523 assumes that you have a full working knowledge of Cadence Analog Design Environment

Instructor: Bertan Bakkaloglu

Welcome to EEE 523!

https://isearch.asu.edu/profile/749234

Contact Info:

Phone: (480) 727-0293

Email: bertan@asu.edu

Office: ISTB4 - 573

Office Hours:

(They would be held via Zoom first three weeks).

Tue/Thu 1pm-2pm AZ

https://asu.zoom.us/j/96213889693

Lab Hours, TA Names and Lab Schedule:

Last Name	First Name	Course	Time	Instructor	LAB TA E-MAIL ADDRESS	LAB TA DUTY TIMES IN LAB AREA
Vignesh	**Aithal**	**EEE 523**	0.50	Bertan Bakkaloglu	vaithal1@asu.edu	TBD

Lab Grader:

Khushbuben Jagdishbhai Vadodariya kvadodar@asu.edu

Course Overview

This course provides a detailed introduction to the design of analog systems, and building blocks, including operational amplifiers, comparators, switched-capacitor circuits. The class will begin with an analysis of monolithic op-amp building blocks, such as common-source, common-gate, and common-drain gain stages and differential pairs. The class follows these fundamental building blocks with operational amplifiers. The amplifiers include folded cascode op-amps, current mirror op-amps, telescopic cascode amplifiers, 2 stage op-amps with various frequency compensation techniques, class AB output stages, fully differential op-amps (and associated common-mode feedback methods), and gain boosting techniques for amplifiers. Bandgap references and comparators will be covered. Noise, input-referred offsets, PSRR+/-, CMRR, and several other non-idealities will be introduced. An introduction to switched capacitor circuits will be studied. There will be a bonus lecture on Phase-Locked-Loops (PLLs) and associated building blocks such as Voltage Controlled Oscillators (VCOs), and Phase-Frequency-Detectors (PFDs).

Course Learning Outcomes

At the completion of this course, students will be able to:

- Demonstrate how to bias fundamental analog building blocks and amplifiers
- Examine methods to generate PTAT/CTAT/Temperature Independent bandgap voltage references
- Explain the design and analysis of various operational-amplifiers
- Identify estimating poles, zeros, and frequency response of complex analog circuits by visual inspection
- Identify fundamentals of phase margin, analog system stability, and Miller frequency compensation
- Explain causes of unwanted signal coupling in analog systems, including power supply rejection, common-mode rejection
- Identify fundamentals of noise analysis in analog systems, including thermal and flicker noise
- Examine design and analysis of class-AB high output current amplification stages
- Develop skills for design and analysis of switched-capacitor analog signal processing systems
- Explain design and analysis of comparators
- Recognize fundamentals of frequency domain analysis of Phase-Locked Loops and associated building blocks

Grading:

3 Projects, total of 45% (15% each)

Midterm1 27.5%

Midterm2 27.5%

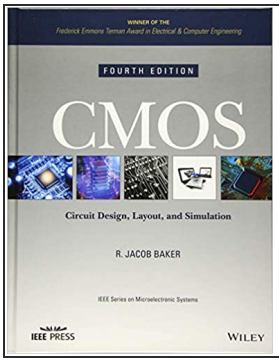
Midterm Dates and Information:

Midterm 1: Tentative: On Thursday, October 13. It will cover from the start of the lectures (Module 1) until the end of (Module 6) bandgap voltage references. Closed books and notes. Calculators are needed, a double-sided cheat sheet is allowed.

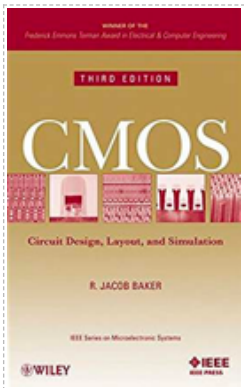
Midterm 2: Tentative: on Tuesday, Nov 22, Starts from noise (Module 7) until the end of switched-capacitor circuits (Module 13) (not including comparators and PLLs, which are bonus lectures). Closed books and notes. Calculators are needed, a double-sided cheat sheet is allowed.

Textbooks

Required

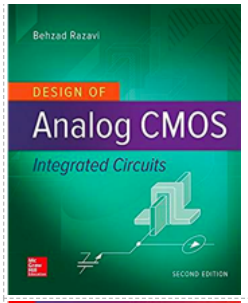
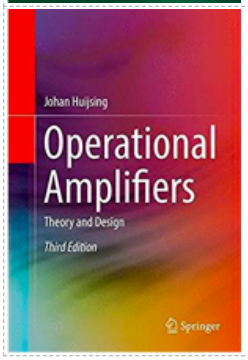
	Baker, J. (2019). CMOS Circuit Design, Layout and Simulation (4th ed.). Piscataway, NJ: Wiley-IEEE Press. ISBN: 978-1-119-48151-5

Optional (earlier edition):

	Baker, J. (2010). CMOS Circuit Design, Layout and Simulation (3rd ed.). Piscataway, NJ: Wiley-IEEE Press.

Optional: For solved examples

	Razavi, B. (2016). Design of Analog CMOS Integrated Circuits (2nd ed.). New York, Ny: McGraw-Hill Education.

	
	Huijsing, J. (2016). Operational Amplifiers: Theory and Design (3rd ed.). New York, NY: Springer.

GWC 273 lab rules to be announced.

Course Access

Your ASU courses can be accessed by both my.asu.edu and myasucourses.asu.edu; bookmark both in the event that one site is down.

Computer Requirements

This is a fully online course; therefore, it requires a computer with internet access and the following technologies:

- Web browsers (Chrome, Mozilla Firefox, or Safari)
- Adobe Acrobat Reader (free)
- Adobe Flash Player (free)
- Webcam, microphone, headset/earbuds, and speaker
- Microsoft Office (Microsoft 365 is free for all currently-enrolled ASU students)
- Reliable broadband internet connection (DSL or cable) to stream videos.

Note: A smartphone, iPad, Chromebook, etc. will not be sufficient for completing your work in ASU Online courses. While you will be able to access course content with mobile devices, you must use a computer for all assignments, quizzes, and virtual labs.

Help

For technical support, use the Help icon in the black global navigation menu in your Canvas course or call the ASU Help Desk at +1-(855) 278-5080. Representatives are available to assist you 24 hours a day, 7 days a week.

Student Success

To be successful:

- check the course daily
- read announcements
- read and respond to course email messages as needed
- complete assignments by the due dates specified
- communicate regularly with your instructor and peers
- create a study and/or assignment schedule to stay on track
- access ASU Online Student Resources

Grading

It will be based on class average and standard deviation.

Submitting Assignments

All assignments, unless otherwise announced, MUST be submitted to the designated area of Canvas. Do not submit an assignment via email.

Assignment due dates follow Arizona Standard time. Click the following link to access the Time Converter to ensure you account for the difference in Time Zones. Note: Arizona does not observe daylight savings time.

Grading Procedure

Grades reflect your performance on assignments and adherence to deadlines. Projects will be available within 2 weeks of the due date via the Gradebook.

Late or Missed Assignments

Notify the instructor **BEFORE** an assignment is due if an urgent situation arises and you are unable to submit the assignment on time.

Follow the appropriate University policies to request an accommodation for religious practices or to accommodate a missed assignment due to University-sanctioned activities.

Communicating With the Instructor

Community Forum

This course uses a discussion topic called "Community Forum" for general questions and comments about the course. Prior to posting a question or comment, check the syllabus, announcements, and existing posts to ensure it's not redundant. You are encouraged to respond to the questions of your classmates.

Email questions of a personal nature to your instructor. You can expect a response within 72 hours.

Questions related to CAD / EDA / Remote Access / Cadence /PDK should be directed to your class TAs.

Chat

The Chat tool in Canvas allows students and teachers to interact in real time. Use Chat only for informal course-related conversations unless your instructor informs you otherwise. Chat is not ideal for questions about assignments; instructors are not required to monitor it and conversations may be buried or lost.

Email

ASU email is an official means of communication among students, faculty, and staff. Students are expected to read and act upon email in a timely fashion. Students bear the responsibility of missed messages and should check their ASU-assigned email regularly.

All instructor correspondence will be sent to your ASU email account.

ASU Online Course Policies

View the ASU Online Course Policies

Accessibility Statements

View the ASU Online Student Accessibility page to review accessibility statements for common tools and resources used in ASU Online courses.

If any other tools are used in this course, links to the accessibility statements will be listed below this sentence.

Topics and Weekly Objectives

Unit or Week	**Topic(s)**	**Weekly Objectives**	**Learning Materials**
1	**Introduction** **and** **Basic MOSFET Operation**	1.1: Introduction and Class Overview 1.2: MOSFET Operation 1.3: Temperature Effects and Design Parameters 1.4 Current Biasing for Analog Design	**Videos:** Section 0 Introduction and Class Overview Section 1 Module 1 Module 2 Module 3 **Book Sections:** Chapter 9.1
2	**Frequency Response and Common Source Amplifiers** **And** **Project 1**	2.1 Temperature and Supply Independent Biasing 2.2 Startup Circuits for Current Biasing 2.3 Cascoded Current Biasing 2.4 Frequency Response of Single Transistor Circuits 2.5 Common Source Amplifiers 2.6 CS Amplifier Design Example	**Videos:** Section 2 Module 1 Module 2 Module 3 Section 3 Module 1 Module 2 Module 3 Project 1 **Book Sections:** Chapter 20

3	**Cascode Amplifiers and Source Followers**	3.1 Common Source Amplifiers (Cont'd.) 3.2 CS Design Example 3.3 Cascode Gain Stages 3.4 Source Followers 3.5 Frequency Response of Source Followers	**Videos:** Section 4 Module 1 Module 2 Section 5 Module 1 Module 2 Module 3 **Book Sections:** Chapter 21
4	**Class AB Output Stages and Differential Amplifiers**	4.1 Output Stages 4.2 Class AB Output Stages 4.3 Differential Amplifiers 4.4 Differential Amplifiers Common Mode Range Analysis 4.5 Differential Amplifiers with a second stage - 2 Stage Design	**Videos:** Section 6 Module 1 Module 2 Section 7 Module 1 Module 2 Module 3 **Book Sections:** Chapter 22
5	**Differential Amplifier Non-Idealities and Telescopic Cascode Amplifiers**	5.1 Common Mode Rejection Ratio Analysis of Amplifiers (CMRR) 5.2 Power Supply Rejection Ratio Analysis of Amplifiers (PSRR +/-) 5.3 Layout Practices for Good Matching 5.4 Telescopic Cascode Amplifiers	**Videos:** Section 8 Module 1 Module 2 Module 3 Module 4 Project 2 **Book Sections:** Chapter 22
6	**Bandgap References**	6.1 Voltage References Overview 6.2 FET Based Current References Revisited 6.3 CTAT Current Generation 6.4 PTAT Current Reference 6.5 Full Bandgap Voltage Reference Design	**Videos:** Section 9 Module 1 Module 2 Module 3 Module 4 Module 5 **Book Sections:** Chapter 23
7	**Noise Analysis of Analog Circuits** **Project 2**	7.1 Noise Analysis 7.2 Noise Modeling in Active Circuits 7.3 Noise Analysis of Amplifiers	**Videos:** Section 10 Module 1 Module 2 Module 3 **Book Sections:** Chapter 8
8	**Two Stage Amplifiers, Stability and Compensation**	8.1 Operational Amplifier Design 8.2 Pole splitting and Stabilization 8.3 Right Hand Plane Zero 8.4 Slew Rate in Amplifiers	**Videos:** Section 11 Module 1 Module 2 Module 3 Module 4 Project 3

			Book Sections: Chapter 24
9	**Folded Cascode and Output Stages**	9.1 Symmetric Amplifiers 9.2 Folded Cascode Amplifiers 9.3 Amplifiers with Output stages	**Videos:** Section 12 Module 1 Module 2 Module 3 **Book Sections:** Chapter 22 & 24
10	**Class AB Output Stages**	10.1 Class AB Operation Revisited 10.2 Class AB Amplifier Distortion 10.3 Class AB Stages Integration into Amplifiers 10.4 Gain Boosting in Amplifiers	**Videos:** Section 13 Module 1 Module 2 Module 3 Module 4 **Book Sections:** Chapter 24
11	**Fully Differential amplifiers and Common Mode Feedback** **Project 3**	11.1 Fully Differential Amplifiers 11.2 Common Mode Feedback	**Videos:** Section 14 Module 1 Module 2 Project 4 **Book Sections:** Chapter 26
12	**Introduction to Switched Capacitor Circuits**	12.1 Switched Capacitor Circuits 12.2 Switched Capacitor Circuits Examples: Sample and Hold Stages 12.3 Switched Capacitor Circuits Examples: SC Filtering 12.4 Deriving Switched Capacitor Integrator Frequency Response	**Videos:** Section 15 Module 1 Module 2 Module 3 Module 4 **Book Sections:** Chapter 25
13	**Switched Capacitor Circuits**	13.1 Deriving Switched Capacitor Integrator Settling Time and OTA Specifications 13.2 Offset Cancellation using Switched Capacitors 13.3 Switched Capacitors Common Mode Feedback 13.4 Fully Differential Amplifiers with SC MFB	**Videos:** Section 15 Module 5 Module 6 Module 7 Module 8 **Book Sections:** Chapter 25 & 26
14	**Comparators**	14.1 Analysis and Design of Analog Comparators	**Videos:** Section 16 Module 1 **Book Sections:** Chapter 27
FINAL WEEK	**Phase Locked Loop Fundamentals**	15.1 Phase locked loop fundamentals 15.2 Voltage Controlled Oscillators (VCOs)	**Videos:** Section 17 Module 1 Module 2 **Book Sections:** Chapter 19

Grading Breakdown

Objective(s)	**Graded**	**Points**	**Due Date**

	Assignments Discussions, quizzes, tests, written assignments		
Unit/Week 2			
	Project 1	15	Week 4
Unit/Week 7			
	Project 2	15	Week 8
Unit/Week 7			
	Midterm 1	27.5	
Unit/Week 11			
	Project 3	15	Week 14
Unit/Week 15			
	Midterm 2	27.5	
		POINT TOTAL: 100	

Syllabus Disclaimer

The syllabus is a statement of intent and serves as an implicit agreement between the instructor and the student. Every effort will be made to avoid changing the course schedule but the possibility exists that unforeseen events will make syllabus changes necessary. Remember to check your ASU email and the course site often.

LAB RULES AND DATES:

EECAD lab information

The EECAD lab in GWC-273 is set to open on August 22nd.

I'll request logins for the EECAD lab classes to be added on August 15th.

Mondays through Thursdays from 9am to 9pm

Fridays from 9am to 6pm (except EEE 202 lab which has a Friday 6pm to 9pm lab session due to high enrollment)

Lab is closed on all Saturdays and Sundays and ASU Holidays

ASU Holidays when GWC 273 lab is closed during fall 2019 semester:

Monday, September 5th, 2022 – Labor Day Holiday

Monday and Tuesday, October 8th and 11th, 2022 – Fall Break

Monday, November 11th, 2022 – Veteran's Day Holiday

Thursday and Friday, November 24th and 25th, 2022 – Thanksgiving Holidays

Final Day of Lab in GWC 273 will be: Friday, December 2th, 2022

All lab exams, lab experiments, lab projects must be finished on or before this date.

Academic Integrity

Students in this class must adhere to ASU's academic integrity policy, which can be found at https://provost.asu.edu/academic-integrity/policy). Students are responsible for reviewing this policy and understanding each of the areas in which academic dishonesty can occur. In addition, all engineering students are expected to adhere to both the ASU Academic Integrity Honor Code and the Fulton Schools of Engineering Honor Code. All academic integrity violations will be reported to the Fulton Schools of Engineering Academic Integrity Office (AIO). The AIO maintains record of all violations and has access to academic integrity violations committed in all other ASU college/schools.

Specific academic integrity rules for this class are…[*You may enter any course specific rules narrative in this section. When discussing sanctions please use language like, *recommended sanctions for these violations will be…*this allows for the fact that the AIO may want to discuss the sanction with you and it also improves the ability to increase the penalty when it is a multiple violation]

Copyright

Course content, including lectures, are copyrighted materials and students may not share outside the class, upload to online websites not approved by the instructor, sell, or distribute course content or notes taken during the conduct of the course (see ACD 304–06, "Commercial Note Taking Services" and ABOR Policy 5-308 F.14 for more information).

You must refrain from uploading to any course shell, discussion board, or website used by the course instructor or other course forum, material that is not the student's original work, unless the students first comply with all applicable copyright laws; faculty members reserve the right to delete materials on the grounds of suspected copyright infringement.

Policy against threatening behavior, per the Student Services Manual, SSM 104–02

Students, faculty, staff, and other individuals do not have an unqualified right of access to university grounds, property, or services. Interfering with the peaceful conduct of university-related business or activities or remaining on campus grounds after a request to leave may be considered a crime. All incidents and allegations of violent or threatening conduct by an ASU student (whether on- or off-campus) must be reported to the ASU Police Department (ASU PD) and the Office of the Dean of Students.

Disability Accommodations.

Suitable accommodations will be made for students having disabilities. Students needing accommodations must register with the ASU disabilities resource Center and provide documentation of that registration to the instructor. Students should communicate the need for an accommodation in sufficient time for it to be properly arranged.

Harassment and Sexual Discrimination

Arizona State University is committed to providing an environment free of discrimination, harassment, or retaliation for the entire university community, including all students, faculty members, staff employees, and guests. ASU expressly prohibits discrimination, harassment, and retaliation by employees, students, contractors, or agents of the university based on any protected status: race, color, religion, sex, national origin, age, disability, veteran status, sexual orientation, gender identity, and genetic information.

Title IX is a federal law that provides that no person be excluded on the basis of sex from participation in, be denied benefits of, or be subjected to discrimination under any education program or activity. Both Title IX and university policy make clear that sexual violence and harassment based on sex is prohibited. An individual who believes they have been subjected to sexual violence or harassed on the basis of sex can seek support, including counseling and academic support, from the university. If you or someone you know has been harassed on the basis of sex or sexually assaulted, you can find information and resources at https://sexualviolenceprevention.asu.edu/faqs.

Mandated sexual harassment reporter: As an employee of the University I am considered a mandated reporter and therefore obligated to report any information regarding alleged acts of sexual discrimination that I am informed of or have a reasonable basis to believe occurred.

ASU Counseling Services, https://eoss.asu.edu/counseling, is available if you wish to discuss any concerns confidentially and privately.