EEE 525: Very Large Scale Integration (VLSI) Design

Spring 2023, MW, 1:30-2:45pm, SCOB 252

Instructor

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Office Hours: TBD

TA TBD

Course Introduction

This course introduces contemporary design of VLSI circuits. The material covers nanometer CMOS technology and scaling, design principles of digital circuits, as well as designs of core VLSI building units. Examples include arithmetic circuits, the memory system, I/O circuitries, and other important circuits for VLSI system integration. Implementations in CMOS will be overarched by considerations of key design metrics, such as timing, power, and reliability, with particular emphasis on low power consumption.

The course is consisted of two components. The first one presents practical design knowledge, including the construction of complex digital design blocks, such as ALU, sequential circuits, and the memory system. The other half will be fundamental design principles, such as the basics of nanoscale CMOS transistor, high-speed design, low-power design essentials, and design for robustness. These principles will govern the implementation and optimization of design units, over a variety of design styles and architecture. The learned knowledge and related tools will be exercised in assignments, using the state-of-the-art 7nm design kits.

This class involves significant design projects using Cadence and Synopsys tools, from RTL design to synthesis and to physical design. These assignments may require up to 30 hours per week of work to complete, depending on your background. Previous experience with these design tools will be helpful.

Prerequisites

This course requires the knowledge of basic CMOS operation, logic gate design, and circuit layout and analysis tools. EEE 425 is the prerequisite.

Text Book

- *CMOS VLSI Design: A Circuits and Systems Perspective*, by Neil H. E. Weste and David Harris, 4th Ed.

Further Reading

- *Design of High-Performance Microprocessor Circuits*, Edited by Anantha Chandrakasan, William J. Bowhill, and Frank Fox. (electronic copy available)
- *Low Power Design Essentials*, by Jan Rabaey, 2009. (electronic copy available)

Grading Policy

The +/- grading system will be used, based on the relative distribution of grades.

Average:	**A-**
Homework (4):	12%
Lab (3+1):	(5%+5%+5%)+20%
Midterm (1):	25%
Final Exam (1):	28%