EEE598 (34761) Special Topic: Semiconductor Heterogeneous Integration

Instructor: Prof. Zhaoyang (Frank) Fan (Zhaoyang.Fan@asu.edu)

Classroom: ECGG237 **Time**: T, Th 4:30-5:45 PM

Objectives: In the post-Moore's Law era of the microelectronics industry, heterogeneous integration (HI) is emerging as the productivity driver of the future. HI uses fine-pitch packaging technology to integrate separately manufactured dissimilar chips (e.g., logic, memory, RF/analog), or components with different materials and functions (e.g., electronic, photonic, and energy devices) into a higher-level system or subsystem in a same 3D system-in-package. Packaging technologies, previously viewed as non-performance enhancing low-value services, now are critical enablers for system performance, to address the demands of "More than Moore." In a broader sense, HI includes the integration of different materials on the same wafer via heteroepitaxial growth, wafer bonding, and other traditional technologies that have been widely used for semiconductor photonics, power electronics, RF/microwave electronics, MEMS, and others.

With enormous investments from the government and the industry to “re-shore” semiconductor manufacturing into the U.S., this is a great time for you to pursue a career in this field. As the industry unanimously agrees that the future of advanced computing will proceed along with HI technologies, this new course “Semiconductor Heterogeneous Integration” will be offered starting spring 2023.

This course is to teach current technologies and disseminate state-of-the-art in this rapidly growing field of microelectronics and microsystems to students who plan to pursue a career in the semiconductor industry, microsystem design, or conducting advanced research in electronics, photonics, and sensor systems. Although this course is more about physical processing, understanding physical implementation is becoming essential for those who plan to become high-level advanced VLSI architects.

Prerequisites: Students in Electrical and Computer Engineering, Physics, Material Science, Chemical Engineering, Mechanical Engineering, and others with basic knowledge of semiconductor processing and semiconductor devices (similar to EEE 436, Fundamentals of Solid-State Devices).

Topics covered (tentatively):

1. Overview of device and system packaging: functions and materials
2. Packaging technology: from System-on-Board to System-in-Package
3. System-on-Chip, challenges of nm-scale device design and processing
4. Chiplet technology and Heterogeneous integration on a substrate
5. Heterogeneous 3D integration
6. Heterogeneous integration of RF, photonic, power, and sensing devices
7. Applications of HI: from smartphones, wearable, to the parallel and edge computing
8. Other topics, new developing trends

Grading:

Class attendance and involvement (10%)

Assignments and Final Learning Report:

~ Bi-Weekly Learning Report (40%)
(summarize the subjects learned in that period, including the reading assignments)

Combined/modified to form Final Learning Report (10%)

Project Report (30%)

Project Presentation (in class or recording) (10%)

>= 98 A+

90-98 A

80-90 B

70-80 C

60-70 D

< 60 F

(These requirements/grading may be adjusted when necessary)