Disclaimer
This syllabus is to be used as a guideline only. The information provided is a summary of topics to be covered in the class.
Information contained in this document such as assignments, grading scales, due dates, office hours, required books and materials may be from a previous semester and are subject to change. Please refer to your instructor for the most recent version of the syllabus.

EEE 120 Digital Design Fundamentals (Hybrid Class) Short Syllabus

Note to the hybrid students:

If you are enrolled in the hybrid section of the course, we will not meet in person on T TH as stated in the course schedule. Instead, the entire class will be Online via Canvas.

Instructor: Bassam Matar

Zoom link: https://asu.zoom.us/j/2986144572

Email: Bassam.Matar@asu.edu (Best method for contacting me!)

Office: GWC 348

Course (Catalog) Description:

Number systems, conversion methods, binary and complement arithmetic, Boolean algebra, circuit minimization, ROMs, PLAs, flipflops, synchronous sequential circuits. Lecture, lab. Cross-listed as CSE 120. Credit is allowed for only CSE 120 or EEE 120.

Textbook: *Introduction to Logic Design, 3nd Ed., Alan B. Marcovitz, McGraw-Hill, 2010* (ISBN-10: 0073191647, ISBN-13: 9780073191645). You could get it from the ASU bookstore or from any 3rd party online source. Just make sure you get the correct edition. The edition provided by the ASU bookstore is the correct edition, even though it sometimes differs in the ISBN.

This book is recommended, not mandatory. The materials we provide should be sufficient for learning and understanding. What is good about this book is the amount of problems at the end of each chapter. While this book is not mandatory since we already provide video lectures and sample and practice problems all over the semester, we highly recommend purchasing this book. Solving a lot of problems is the key to mastering this class.

Supplemental Materials: Laboratory Manual available on Canvas, "Digital" software (available for free). No Hardware kits needed for this class.

Course Objective:

Students will be able to analyze, design, construct, and debug digital combinational logic circuitry and digital finite state machine circuitry.

Course Outcomes:

- 1. Students will be able to describe the function of electric circuits that perform logic operations using symbols for logic gates or input/output tables (truth tables).
- 2. Students will be proficient in the use of algebraic equations to describe and analyze Digital Logic circuits and use Boolean Algebra to simplify the circuits.
- 3. Students will be able to perform algebraic operations in different number systems (as opposed to the traditional decimal system)
- 4. Students will be able to design, build, debug, and demonstrate the operation of arbitrarily complex combinational Digital Logic circuits.
- 5. Students will be able to design, build, debug, and demonstrate the operation of arbitrarily complex synchronous machines given a reasonable problem statement.
- 6. Students will be able to set criteria to determine the "best" design and select the best design.
- 7. Students will be able to describe the operation of an elementary microprocessor, create an instruction set for an elementary microprocessor, and enter the instruction set into the processor's instruction PROM. Students will also be able to enter a program in the processor's memory and execute the program.

Course Details:

This course is divided into 8 Modules, each spans 1 week except for Module 8 which is usually 2 days depending on the ASU academic calendar. The course has a total of 1000 points excluding the extra-credit points. The Modules in this class are as follows:

- 1. Module 1 Electrical Circuit Fundamentals, Logic Circuit Description, Truth Tables
- 2. Module 2 Number Systems, Addition and Subtraction, 2's Complement
- 3. Module 3 Boolean Algebra, Logic Minimization, Karnaugh Maps
- 4. Module 4 Advanced Combinational Logic: Multiplexers, Decoders, Programmable Logic
- 5. Module 5 Sequential Logic: Latches, Flip Flops, Registers, Counters
- 6. Module 6 Synchronous Finite State Machine Design
- 7. Module 7 Microprocessor Design
- 8. Module 8 Final Exam Review (usually this module is less than one week)

Laboratory Experiments:

In a set of five stages (labs), students use digital logic simulation software to simulate a simple microprocessor. They start with simple boolean gates, build and simulate the microprocessor parts including an ALU. Memory is then added and in the final stage the students develop machine code instructions for the microprocessor. Reports are due after each stage.

The five laboratory expirements and the capstone project are in the following order:

- Lab 0 (Module 1): Simulator Tutorial: How to use the lab Software
- Lab 1 (Module 2): Half Adder, Increment and 4-Bit Full Adder
- Lab 2 (Module 3): Multiplexer, Decoder, the Arithmetic and Logic Unit and 7-Segment Display
- Lab 3 (Module 4): The Brainless Microprocessor
- Lab 4 (Module 5): The Complete Microprocessor
- Capstone design project

Course Contribution to Engineering Science and Design:

On tests students will be presented with problems that require them to design digital logic system based on first principles. In addition the Capstone Design Project requires students to design, implement and test a finite state machine solely based on end user requirements. The students should be able to come up with an independent design and come up with solutions to issues arising, e.g. need for synchronization of input or output signals. By applying analytical tools, students are able to verify that their design performs according to the specifications. The students are graded on presenting a circuit that performs the application.

Course Relationship to Program Objectives:

This course, through work required of our students (i.e., homework, exams/quizzes, and laboratory assignments) supports the following objectives of our program (ABET a,b,c,d,g,k):

Being the first course in the Digital Design undergraduate curriculum, students will be introduced to the mathematical fundamentals of logic design and logic minimization (a).

Students will learn about essential building blocks of modern Digital Logic Systems such as Multiplexers and Decoders and Programmable Logic Devices. They will also be introduced to sequential logic design which is the fundamental concept behind shift regiters and counters. These in turn make up vital parts of modern Digital Systems employing State Machine Design. Students will conduct experiments that will help to reinforce what has been learned through analysis and interpretation of the data observed (b). Equipped with this knowledge, students will design components of larger Digital Systems, such as an Arithmetic Logic Unit as part of a Microprocessor (c). Students will also be involved in a Capstone project which requires each individualstudent to design a Finite State Machine and document the design process. Thus, the course enhances the individual communication skills (g) as well as fosters collaborative work on multidiciplinary teams though group excercises and discussions (d). Modern CAD software tools are employed in homework, labs, and the Capstone project to design, analyze, and evaluate designs (k,c).

Lab Software:

The lab software we will use for this semester is called "Digital". We will provide you with the installation package for this software to work on your computer (Windows or Mac). Do not try to download any versions of this software from the internet. To be consistent with all students, we will share with you the correct version when the class starts.

Lab FAQs:

2- What system requirements will I need for the software needed for this class?

The Digital software will be compatible with most Windows-based and Mac-based computers (desktop or laptop). Installation instructions will be provided for both.